ABSTRACT OF THE DISCLOSURE

A method and apparatus for performing block sequential processing is described. In one embodiment, the apparatus comprises a determine pass logic, selection logic, next coefficient logic and control. The determine pass logic has inputs coupled to receive significance state information for a region, a pass bit for each coefficient in a subset of the region, and a current pass indication. In response to these inputs, the determine pass logic generates pass indications to indicate a pass for each coefficient in the subset of the region. The selection logic has inputs coupled to signals output from the determine pass logic and the current pass indication and, in response to these inputs, generates output indications associated with one pass of either the significance propagation, refinement, and cleanup passes. The next coefficient logic is coupled to the selection logic and indicates the next coefficient in the current pass in response to the output indications from selection logic. The control is coupled to receive the output indicating the next coefficient in the one pass and codes coefficients in the significance propagation, refinement and cleanup passes. The control also codes the next coefficient in either the significance propagation, refinement and cleanup passes as indicated by the next coefficient logic.